WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

providing a silicon-containing substrate, having an upper surface, comprising: a gate electrode formed on the upper surface of the substrate with a gate insulating layer therebetween, the gate electrode having an upper surface and opposing side surfaces, and source/drain regions in the substrate spaced apart from the gate electrode;

forming supersaturated dopant concentration source/drain extensions in the substrate between the source/drain regions and the gate electrode; and

forming metal silicide contacts on the upper surfaces of the gate electrode and the substrate, in a manner sufficient to maintain the supersaturated dopant concentration in the source/drain extensions

2. The method according to claim 1, wherein the temperatures is maintained below about 700°C throughout the forming of the metal silicide contacts.

3. The method according to claim 2, wherein the metal silicide contacts are made of NiSi.

4. The method according to claim 3, wherein the silicon containing substrate further comprises sidewall spacers on the gate electrode opposing side surfaces, the method further comprising forming source/drain regions and subsequently removing the sidewall spacers prior to forming the source/drain extensions.

5. The method according to claim 3, wherein the step of forming the metal silicide contacts comprises:

depositing a dielectric layer over the substrate and gate electrode upper surfaces;

patterning the dielectric layer to form sidewall spacers on the gate electrode opposing side surfaces;

depositing a nickel layer over the gate electrode upper surface, sidewall spacers, and substrate upper surface;

heating to react the nickel layer with underlying silicon in the gate electrode and source/drain regions to form the nickel silicide (NiSi) contacts;

and removing the nickel that did not react to form nickel silicide.

6. The method according to claim 3, wherein the nickel layer is heated at a temperature of about 400°C to about 600°C for about 15 seconds to about 120 seconds to form the NiSi contacts.

7. The method according to claim 3, wherein the dopant concentration in the source/drain extensions is about 10^{21} ions/cm^3.

8. The method according to claim 3, wherein the step of forming the supersaturated source/drain extensions comprises:

ion implanting a dopant; and

exposing the dopant implants to laser radiation at an energy density sufficient to anneal the dopant implants.

9. The method according to claim 8, wherein the source/drain extensions are formed at an ion implantation dosage of about $1x10^{14}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2 and an ion implantation energy of about 1 keV to about 50 keV, and with a laser radiation energy density of about 0.1 J/cm^2 to about 5.0 J/cm^2.

10. The method according to claim 3, wherein the step of forming the supersaturated source/drain extensions comprises forming the source/drain extensions by doped selective epitaxy.

11. The method according to claim 10, wherein the step of forming the source/drain extensions by doped selective epitaxy comprises:

forming an oxide layer on the semiconductor substrate and gate electrode;

patterning the oxide layer to form an oxide film on the gate opposing side surfaces;

forming an epitaxial layer by applying a gas mixture comprising SiH_4, and a dopant gas to the substrate surface at a temperature of about 700°C to about 900°C and at a pressure of about 1 torr to about 700 torr.

12. A method of manufacturing a semiconductor device, the method comprising:

providing a silicon-containing semiconductor substrate;

forming a gate oxide layer on the semiconductor substrate;

forming a conductive gate material layer over the gate oxide layer;

patterning the gate material layer and gate oxide layer to form a gate electrode having an upper surface and opposing side surfaces, with a gate oxide layer thereunder;

depositing a layer of insulating material over the gate electrode and semiconductor substrate;

patterning the insulating material to form sidewall spacers on the opposing side surfaces of the gate electrode;

forming source/drain regions by ion implanting a dopant into the substrate;

removing the sidewall spacers;

heating the substrate to activate the source/drain regions;

forming supersaturated dopant concentration source/drain extensions between the gate electrode and source/drain regions;

depositing a second layer of insulating material over the gate electrode and semiconductor substrate;

patterning the second layer of insulating material to form sidewall spacers on the opposing side surfaces of the gate electrode;

depositing a metal layer over the gate electrode upper surface, sidewall spacers, and substrate upper surface;

heating at a temperature to react the metal layer with underlying silicon to form metal silicide contacts on the gate electrode and substrate upper surfaces without reducing the dopant concentration in the source/drain extensions below a supersaturated dopant concentration; and

removing the metal that did not react to form metal silicide.

13. The method according to claim 12, wherein the metal layer is Ni.

14. The method according to claim 13, wherein the supersaturated source/drain extensions are formed by doped selective epitaxy.

15. The method according to claim 14, wherein the step of forming the source/drain extensions by doped selective epitaxy comprises;

forming an oxide layer on the gate electrode and semiconductor substrate;

patterning the oxide layer to form an oxide film on the gate electrode opposing side surfaces;

forming an epitaxial layer on the substrate by applying a gas mixture comprising SiH_4 and a dopant gas to the substrate surface at a temperature of about 700°C to about 900°C and at a pressure of about 1 torr to about 700 torr.

16. The method according to claim 13, wherein the step of forming the supersaturated source/drain extension comprises:

ion implanting a dopant; and

exposing the dopant implants to laser radiation at an energy density sufficient to anneal the dopant implants.

17. The method according to claim 16, wherein source/drain extensions are formed at an implantation dosage of about $1x10^{14}$ ions/cm^2 to about $1x10^{16}$ cm^2 and an ion implantation energy of

about 1 keV to about 50 keV, and with a laser radiation energy density of about 0.1 J/cm^2 to about 5.0 J/cm^2.

18. The method according to claim 13, wherein the dopant concentration in the source/drain extensions is about 10^{21} ions/cm^3.

19. A semiconductor device comprising:

a silicon-containing substrate, having an upper surface;

a gate electrode formed on the substrate upper surface with a gate insulating layer therebetween, the gate electrode having an upper surface and opposing side surfaces;

source/drain regions formed in the substrate spaced apart from the gate electrode;

source/drain extensions formed in the substrate between the source/drain regions and the gate electrode, wherein the source/drain extensions contain a supersaturated dopant concentration; and

metal silicide contacts formed on the gate electrode and substrate upper surfaces.

20. The semiconductor device of claim 19, wherein the metal silicide is NiSi.